

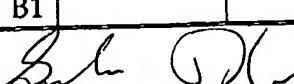


ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Symbolic model checking with dynamic model pruning						
Application Number:	10/666619						
Confirmation Number:	6808						
First Named Applicant:	Jin Yang						
Attorney Docket Number:	42P8534C						
Art Unit:	2825						
Examiner:	Annette Thompson						
Search string:	(5870509 or 6484134).pn.						
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5870509	1999-02-09	Kita et al.			
S.P.	2	6484134	2002-11-19	Hoskote			
Signature							
Examiner Name				Date			
				3-6-06			

Substitute for Form 1449A/PTO (Modified)			Attorney Docket No.: 42P8534C	Application Number: Unassigned 10-666619		
Sheet 1 of 4			First Named Inventor: Jin Yang	Examiner: Unassigned		
			Filing Date: Herewith	Art Unit: Unassigned		
U.S. PATENT DOCUMENTS						
Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
S.P.		5,119,318		Paradies et al.	06/02/1992	
S.P.		5,481,717		Gaboury	01/02/1996	
S.P.		5,469,367		Puri et al	11-21-1995	
S.P.		5,491,639		Filkorn	02-13-1996	
S.P.		5,594,656		Tamisier	01-14-1997	
S.P.		5,691,925		Hardin et al.	11/25/1997	
S.P.		5,754,454		Pixley et al	05-19-1998	
S.P.		5,768,498		Boigelot, et al	06-16-1998	
S.P.		5,905,977		Goubault	05-18-1999	
S.P.		5,937,183		Ashar et al	06-10-1999	
S.C.		6,026,222		Gupta et al	02-15-2000	
S.P.		6,035,109		Ashar et al	03-07-2000	
S.P.		6,086,626		Jain et al	07-11-2000	
S.P.		6,131,078		Plaisted	10-10-2000	
S.P.		6,148,436		Wohl	11-14-2000	
S.P.		6,185,516		Hardin et al	02-06-2001	
S.P.		6,209,120		Kurshan et al	03-27-2001	
S.P.		6,247,165		Wohl et al	06-12-2001	
S.P.		6,292,916		Abramovici et al	09-18-2001	
S.P.		6,301,687		Jain et al	10-09- 2001	
S.P.		6,308,299		Burch et al	10-23- 2001	
S.P.		6,321,186		Yuan et al	11-20- 2001	
S.P.		6,339,837		Li	01-15-2002	
S.P.		6,341,367	B1	Downing	01/22/2002	
Examiner Signature					Date Considered 2/22/06	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

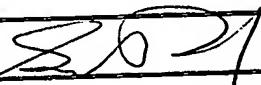
¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. 'Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). 'For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. 'Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 'Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42P8534C	Application Number: Unassigned
Sheet 2 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: Herewith	Art Unit: Unassigned

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
S.R.		BEREZIN, S. et al, "A Compositional Proof System for the Modal μ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University, January 15, 1997</i>	
S.R.		BEREZIN, S. et al, "Model Checking Algorithms for the μ -Calculus," <i>Technical Report CMU-CS-96-180, Carnegie Mellon University, September 23, 1996</i>	
S.R.		BRADLEY, J. et al, "Compositional BDD Construction: A Lazy Algorithm," <i>Dept. of Computer Science, University of Bristol, April 1998</i> , pages 1-8.	
S.R.		BRYANT, R. E. et al, "Formal Hardware Verification by Symbolic Ternary Trajectory Evaluation," <i>28th ACM/IEEE Design Automation Conference, Paper 24.2, 1991</i> , pages 397-402	
S.R.		BRYANT, R. E., "Binary Decision Diagrams & Beyond," <i>Tutorial at ICCAD '95, Carnegie Mellon University, 1995</i>	
S.R.		BURCH, J. R. et al, "Representing Circuits More Efficiently in Symbolic Model Checking," <i>28th ACM/IEEE Design Automation Conference, Paper 24.3, 1991</i> , pages 403-407	
S.R.		BURCH, J. R. et al, "Sequential Circuit Verification Using Symbolic Model Checking," <i>27th ACM/IEEE Design Automation Conference, Paper 3.2, 1990</i> , pages 46-51	
S.R.		BURCH, J. R. et al, "Symbolic Model Checking for Sequential Circuit Verification," <i>IEEE Transactions on Computer-Aided Design for Integrated Circuits and Systems, April 1994</i> , pages 401-424	
S.R.		CAMPOS, S., "Real-Time Symbolic Model Checking for Discrete Time Models," <i>Technical Report CMU-CS-94-146, Carnegie Mellon University, Pittsburgh, PA, May 2, 1994</i>	
S.R.		CAMPOS, S., "Symbolic Model Checking in Practice," <i>IEEE Proceedings, XII Symposium on Integrated Circuits and System Design, Oct 2, 1999</i> , pages 98-101.	
S.R.		CHAN, W. et al, "Combining Constraint Solving and Symbolic Model Checking for a Class of Systems with Non-linear Constraints, <i>Computer Aided Verification, 9th International Conference, CAV '97 Proceedings (O. Grumberg, Editor)</i> , Lecture Notes in Computer Science 1254, pages 316-327, Haifa, Israel, June 1997. Springer-Verlag (Revised in December '98)	
S.R.		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University, May 1997</i>	

Examiner Signature		Date Considered	2/22/06
--------------------	---	-----------------	---------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42P8534C	Application Number: Unassigned
Sheet 3 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: Herewith	Art Unit: Unassigned

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
SQ		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability Analysis," <i>ACM Transactions on Software Engineering and Methodology</i> , Vol. 8, No. 1, January 1999, pages 49-78	
SQ		CHIODO, M. et al, "Automatic Compositional Minimization in CTL Model Checking," <i>Proceedings of 1992 IEEE/ACM International Conference on Computer-Aided Design</i> , November, 1992, pages 172-178	
SQ		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," <i>International Conference on Computer-Aided Verification(CAV'99)</i> , Trento, Italy, July 1999 pp. 196-207, Proceedings of CAV'99, Lecture Notes in Computer Science #1633 (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlog, 1999	
SQ		CLARKE, E. et al, "Another Look at LTL Model Checking," <i>Technical Report CMU-CS-94-114, Carnegie Mellon University</i> , February 23, 1994	
SQ		CLARKE, E. et al, "Combining Symbolic Computation and Theorem Proving: Some Problems of Ramanujan," <i>Technical Report CMU-CS-94-103, Carnegie Mellon University</i> , January 1994	
SQ		CLARKE, E. M. et al, "Formal Methods: State of the Art and Future Directions," <i>ACM Computing Surveys</i> , Vol. 28, No. 4, December 1996, pages 626-643	
SQ		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 343-354	
SQ		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>ACM Transactions on Programming Languages and Systems</i> , Vol. 16, No. 5, September 1994, pages 1512-1542	
SQ		GRUMBERG, O., "Model Checking and Modular Verification," <i>ACM Transactions On Programming Languages and Systems</i> , Vol. 16, No. 3, May 1994, pages 843-871	
SQ		Hojati, R. et al, "Early Quantification and Partitioned Transition Relations," <i>Proceedings, IEEE International Conference on Computer Design: VLSI in Computers and Processors</i> , Oct. 9, 1996, pages 12-19	
SQ		JACKSON, D., "Exploiting Symmetry In the Model Checking of Relational Specifications," <i>Technical Report CMU-CS 94-219, Carnegie Mellon University</i> , December 1994	

Examiner Signature		Date Considered	2/22/06
--------------------	---	-----------------	---------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42P8534C	Application Number: Unassigned
Sheet 4 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: Herewith	Art Unit: Unassigned

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
S.Q.		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," <i>Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design</i> , pp. 109-125, November 1996	
S.Q.		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," <i>Carnegie Mellon University Ph.D. Dissertation</i> , July 1997	
S.Q.		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," <i>Proceedings of the 32nd ACM/IEEE Conference on Design Automation</i> , January 1995	
S.Q.		JHA, S. et al, "Equivalence Checking Using Abstract BBDs," <i>Technical Report CMU-CS-96-187, Carnegie Mellon University, Pittsburgh, PA</i> , October 29, 1996	
S.Q.		KERN, C. et al, "Formal Verification In Hardware Design: A Survey," <i>ACM Transactions on Design Automation of Electronic Systems</i> , Vol. 4, No. 2, April 1999, pages 123-193	
S.Q.		KURSHAN, R. et al, "Verifying Hardware in its Software Context," <i>Proceedings of the 19th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 742-749	
S.Q.		NELSON, K. L. et al, "Formal Verification of a Superscalar Execution Unit," <i>34th Design Automation Conference</i> , June 1997	
S.Q.		TUYA, J. et al, "Using a Symbolic Model Checker for Verify Safety Properties in SA/RT Models," <i>Proceeding of the 5th European Software Engineering Conference, Lecture Notes in Computer Science</i> , Vol. 989, Springer-Verlag, Berlin, 1995, pages 59-75	
S.Q.		VELEV, M. N., "Efficient Modeling of Memory Arrays in Symbolic Simulations," <i>Proceedings of Computer-Aided Verification</i> , June 1997	
S.Q.		WING, J. M. et al, "A Case Study in Model Checking Software Systems," <i>Technical Report CMU-CS-96-124, Carnegie Mellon University, Pittsburgh, PA</i> , April 1996	
S.Q.		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," <i>28th ACM/IEEE Design Automation Conference</i> , 1991	
S.Q.		Zhang Z., "An Approach to Hierarchy Model Checking via Evaluating CTL Hierarchically," <i>IEEE Proceedings of the Fourth Asian Test Symposium</i> , Nov. 24, 1995, pages 45-49.	

Examiner Signature	<i>SQ</i>	Date Considered	2/22/06
--------------------	-----------	-----------------	---------

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.